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... as a sequence of WRITE-INVALIDATE trans ... themselves naturally to a multithreaded software

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architecture ... accesses to DRAM: (a) microengine thread writes descriptor ...

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G Komaros, T Orphanoudakis, N Zervos, E ... - [ieeexplore.ieee.org](#)

... mechanism, than on associating one micro-engine to the ... network processor ([7]) uses

256 threads in eight ... et al, 'A Massively Multithreaded Packet Processor ...

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to move packets from a microengine only to its neighboring micro- engine. ...

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... Six 32-bit, multithreaded RISC data engines (microengines ... The hardware-based

multithreading enables other threads ... Then, the microengine thread would use PCI DMA ...

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BO Technology - [cse.iitb.ac.in](#)

... The Microengines utilize a feature called Hardware Multithreading. Each Microengine

has four Program Counters, and supports ... Each thread has its own Thread ID ...

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L George, M Blume - Proceedings of the ACM SIGPLAN 2003 conference on ..., 2003 - [portal.acm.org](#)

... 3.3 Exposing Hardware Features The IXP microengine instruction set is ... Examples include

inter- thread communication (on the same micro-engine, on different mi ...

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[Development of a new hardware-in-loop simulation platform for GD-1 diesel engine based on can and ...](#)

J Wang, H Tang, K Zhu, L Yang, X Mao, B Zhuo - Vehicular Electronics and Safety, 2005. IEEE International ..., 2005 - [ieeexplore.ieee.org](#)

... c++ and ran in the background as sub threads. ... HIL simulation platformn based on

multithread and CAN ... be used as a dedicated micro-engine operating independently ...

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[Building a robust packet control unit with network processors](#)

TOC View - Embedded Software and Systems, 2005. Second International ..., 2005 - [ieeexplore.ieee.org](#)

... are achieved through an innovative micro- engine architecture that ... Each microengine

has eight threads, and each thread has ... refers to a set of threads which are ...

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[A highly flexible, distributed multiprocessor architecture for network processing - group of 6 »](#)

M Venkatachalam, P Chandra, R Yavatkar - Computer Networks, 2003 - Elsevier

... ME provides support for software con- trolled multithreaded operation ... 4. Microengine

programming model ... order can be maintained using ordered thread execution or ...

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[Design and Implementation of a Network Processor Input/Output Module - group of 3 »](#)

I Sourdis - [mhl.tuc.gr](#)

... The device operates at 166 MHz. Each micro-engine supports 4 threads, which helps

to ... Microengine Core Speed 166 MHz 200 MHz 232 MHz 166 MHz extended temp ...

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[Method and apparatus for gigabit packet assignment for multithreaded packet processing - group of 3 »](#)

G Wolrich, D Bernstein, MJ Adiletta, DF Hooper - US Patent 6,661,794, 2003 - Google Patents
... 376 Write MPKTsequence no. ... thread) Page 21. enqueue ... US 6,661,794 BI METHOD AND APPARATUS
FOR GIGABIT PACKET ASSIGNMENT FOR MULTITHREADED PACKET PROCESSING ...
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G Wolrich, D Bernstein, MJ Adiletta, W Wheeler - US Patent 6,532,509, 2003 - Google Patents
... the hardware-based multithreaded processor 12 ... general, the hardware-based multi-
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G Wolrich, D Bernstein, MJ Adiletta, W Wheeler - US Patent 6,587,906, 2003 - Google Patents
... the hardware-based multithreaded processor 12 ... general, the hardware-based multi-
threaded processor 12 ... completion signal to the initiating microengine thread. ...
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[Solving parallel problems employing hardware multi-threading in a parallel processing environment - group of 3 »](#)

G Wolrich, WR Wheeler, MJ Adiletta - US Patent 6,629,237, 2003 - Google Patents
... of the hardware-based multithreaded processor 12 ... Advantages of hardware multithreading
can be explained by ... from one of the micro engine thread contexts reports ...
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[Port blocking technique for maintaining receive packet ordering for a multiple ethernet port switch - group of 2 »](#)

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... 1-5. "Nomadic Threads: A migrating multithread approach to remote memory ... 20-23, 1996.
"Overview of the START ("T) multithreaded computer" by Beckerie, MJ ...
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DF Hooper, MJ Adiletta, GM Wolrich - US Patent 6,952,824, 2005 - Google Patents
... 141-152, 1996 IEEE.* Vibhatvanij, K. Simultaneous Multithreading-Based Rout ...
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H Krawczyk, T Madajczak - Parallel Computing in Electrical Engineering, 2004. ..., 2004 - ieeexplore.ieee.org
... covered all coherency problems for multithreaded multiengine processor ... implemented
if a single microengine does not ... caused by an unordered thread entering into ...
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Ensuring data integrity by locked-load and conditional-store operations in a multiprocessor system - group of 2 »

RL Sites, RT Witek - US Patent 5,193,167, 1993 - Google Patents

... of previously-established data structures, include the facility for doing in-register **byte** extract, insert and masking, along with non-aligned **load** and store ...

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System for handling load and/or store operations in a superscalar microprocessor - group of 3 »

CD Senter, J Wang - US Patent 5,557,763, 1996 - Google Patents

... 25!, i v r20i i! **LOAD STQR** UNIT HSU] i i i ... ADDRESSIJ[3: 0] 41 VÂLD213 424 y-MASK 475 ADDRESS2_3[3: 0] cmpmejb ... ADDRESS: **BYTE**: XXXXXX5 4 FIG. 6 ...

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VIS speeds new media processing - group of 3 »

M Tremblay, JM Narayanan, VL He - Micro, IEEE, 1996 - [ieeexplore.ieee.org](#)

... address in pst as sldfa..ASLPST8P Parial-sture instruc ion using **mask** in lid ... 2/1 ifld) 1/1(1st) bid, bst i/is stdfa ,ASLBLK_P 64-**byte** block **load** or store ...

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The Visual Instruction Set (VIS) in UltraSPARCm - group of 4 »

L Kohn, G Maturana, M Tremblay, A Prabhu, G Zyner - Proceedings of COMPCON, 1995 - [doi.ieeecomputersociety.org](#)

... The different versions gen- erate **masks** for 8-, 16-, or ... and store instructions transfer one or two **bytes** of memory ... The data from a **load** is zero-extended in the ...

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Reducing the performance impact of instruction cache misses by writing instructions into the ... - group of 5 »

J Stark, P Racunas, YN Patt - Proceedings of the 30th annual ACM/IEEE international ..., 1997 - [portal.acm.org](#)

... it will need to know how the architectural **destination** registers were ... address of both the store and **load** are known ... of- order issue with a 12k **byte mask** cache is ...

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Register Packing: Exploiting Narrow-Width Operands for Reducing Register File Pressure - group of 11 »

O Ergin, D Balkan, K Ghose, D Ponomarev - Proceedings of the 37th International Symposium on ..., 2004 - [portal.acm.org](#)

... the data-width predictors similar to the **load** value predictor ... well as the sign extension and **byte** multiplexing logic ... to include the parts bit-**mask** (Section 3.2 ...

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In-register data manipulation using data shift in reduced instruction set processor - group of 3 »

RL Sites, RT Witek - US Patent 5,367,705, 1994 - Google Patents

... The instruction set is limited to **register-to-register** operations and regis- ter **load/store** operations. **Byte** manipulation instruc- tions, included to permit ...

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Register scorbarding on a microprocessor chip - group of 2 »

D Budde, R Riches, MT Imel, G Myers, K Lai - US Patent 4,891,753, 1990 - Google Patents

... Each pending **load** operation is associated with a **mask** ... for memory accesses, one method for **byte-move** operations ... Each matchcell looks at 40 one **mask** from the ...

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In-register data manipulation for unaligned byte write using data shift in reduced instruction set ... - group of 3 »

RL Sites, RT Witek - US Patent 5,410,682, 1995 - Google Patents

... **Byte** manipulation instruc- tions, included to permit use ... the facility for doing in-**register** byteextract, insertandmasking ... along withnon-aligned **load** and store ...

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[Digital computer system with cache controller coordinating both vector and scalar operations - group of 2 »](#)

JP Ellis, E Nangia, N Patwa, B Shah, GM Wolrich - US Patent 5,418,973, 1995 - Google Patents

... VECTOR LENGTH REGISTER (VLR) VECTOR MASK REGISTER (VMR) VECTOR COUNT REGISTER (VCR) ... arithmetic pipes, one for the pipe **destination**, a load ...

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